AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application:

Listing of Claims:

Claim 1. (currently amended): An oscillator circuit, comprising:

a voltage controlled oscillator having an inductor and a variable capacitor configured to generate an output signal having a frequency of n times of a target frequency;

a PLL synthesizer having a programmable counter, a phase detector and a control voltage generation circuit, wherein the programmable counter divides an output signal of the voltage controlled oscillator, the phase detector is configured to detect phase difference between the output signal from the ~~voltage controlled oscillator~~ programmable counter and a reference signal, and the control voltage generator circuit is configured to generate a control signal of the voltage controlled oscillator based on the phase information detected at the phase detector so that the voltage controlled oscillator is controlled to generate the output signal having a frequency of n times of [[a]] the target frequency,

a frequency divider circuit provided separately from the PLL synthesizer, dividing the output signal from the voltage controlled oscillator into 1/n frequency and generating at least two signals having an equal frequency and different phases by 180° from each other,

wherein a frequency of the voltage controlled oscillator is controlled to be a frequency n times a target frequency so that it is possible to form the inductor and the capacitor of the voltage controlled oscillator on a semiconductor IC, a division ratio of the frequency divider circuit is set to be 1/n so that a frequency of the output signal of the voltage controlled oscillator is made to be

1/n, and the voltage controlled oscillator, the PLL synthesizer, and the frequency divider circuit are formed on a semiconductor integrated circuit [[board]].

Claim 2. (currently amended): An oscillator circuit, comprising:

a voltage controlled oscillator having an inductor and a variable capacitor configured to generate an output signal having a frequency of n times of a target frequency;

a PLL synthesizer having a first frequency divider, a phase detector and a control voltage generation circuit, wherein the first frequency divider is configured to divide an output signal from the voltage controlled oscillator, the phase detector is configured to detect phase difference between the output signal from the first divider and a reference signal, and the control voltage generator circuit is configured to generate a control signal of the voltage controlled oscillator based on the phase information detected at the phase detector so that the voltage controlled oscillator is controlled to generate the output signal having a frequency of n times of [[a]] the target frequency,

a second frequency divider circuit provided separately from the PLL synthesizer, dividing the output signal from the voltage controlled oscillator into 1/n frequency and generating at least two signals having an equal frequency and different phases by 180° from each other,

wherein a frequency of the voltage controlled oscillator is controlled to be a frequency n times a target frequency so that it is possible to form the inductor and the capacitor of the voltage controlled oscillator on a semiconductor IC, a division ratio of the frequency divider circuit is set to be 1/n so that a frequency of the output signal of the voltage controlled oscillator is made to be 1/n, and the voltage controlled oscillator, the PLL synthesizer, and the second frequency divider circuit are formed on a semiconductor integrated circuit [[board]].

Claim 3. (previously presented): The oscillator circuit in claim 1, wherein said oscillating unit comprises a plurality of MOSFETs, an inductance and a variable capacitance element.

Claim 4. (original): The oscillator circuit in claim 2, wherein said oscillating unit comprises a plurality of MOSFETs, an inductance and a variable capacitance element, and said control voltage generation circuit controls an oscillation frequency of the oscillating unit by outputting a control voltage to the variable capacitance element for changing the capacitance of the variable capacitance element.

Claim 5. (previously presented): The oscillator circuit in claim 1 wherein said oscillating unit comprises a first and a second MOSFETs, an inductance and a variable capacitance element;

either the source or drain of the first MOSFET is connected with the inductance and the variable capacitance element; the gate of the first MOSFET is connected with the source or drain of the second MOSFET; and the gate of the second MOSFET is connected with the source or drain of the first MOSFET.

Claim 6. (previously presented): The oscillator circuit in claim 1, wherein said oscillating unit comprises a first and a second MOSFETs, an inductance, a capacitor and a variable capacitance element;

either the source or drain of the first MOSFET is connected with the inductance, the gate of the first MOSFET is connected with either the source or drain of the second MOSFET, the gate of the second MOSFET is connected with either the source or drain of the first MOSFET, and either the source or drain of the first MOSFET is connected with the variable capacitance element by way of the capacitor; and

a control voltage outputted from said control voltage generation circuit is applied to the variable capacitance element so as to change the capacitance thereof and thereby controlling an oscillation frequency.

Claim 7. (previously presented): The oscillator circuit in claim 1, wherein said variable capacitance element comprises a MOSFET.

Claim 8. (previously presented): The oscillator circuit in claim 1, wherein a control voltage generation circuit detects a phase difference between a divided signal of a signal generated by said oscillating unit and a reference signal, and outputs a control voltage according to the phase difference.

Claim 9. (previously presented): The oscillator circuit in claim 1, wherein said control voltage generation circuit is a PLL synthesizer circuit comprising a programmable counter, a phase detection circuit comparing phases between a signal outputted from the programmable counter and the reference signal, and a low-pass filter blocking a high frequency component of an output signal of the phase detection circuit and outputting a DC control voltage to said oscillating unit.

Claim 10. (previously presented): The oscillator circuit in claim 1, wherein said divider circuit includes a divider circuit having a duty ratio of 50%.

Claim 11. (previously presented): The oscillator circuit in claim 2, wherein said oscillating unit comprises a plurality of MOSFETs, an inductance and a variable capacitance element.

Claim 12. (previously presented): The oscillator circuit in claim 2 wherein said oscillating unit comprises a first and a second MOSFETs, an inductance and a variable capacitance element;

either the source or drain of the first MOSFET is connected with the inductance and the variable capacitance element; the gate of the first MOSFET is connected with the source or drain of the second MOSFET; and the gate of the second MOSFET is connected with the source or drain of the first MOSFET.

Claim 13. (previously presented): The oscillator circuit in claim 2 wherein said oscillating unit comprises a first and a second MOSFETs, an inductance, a capacitor and a variable capacitance element;

either the source or drain of the first MOSFET is connected with the inductance, the gate of the first MOSFET is connected with either the source or drain of the second MOSFET, the gate of the second MOSFET is connected with either the source or drain of the first MOSFET, and either the source or drain of the first MOSFET is connected with the variable capacitance element by way of the capacitor; and

a control voltage outputted from said control voltage generation circuit is applied to the variable capacitance element so as to change the capacitance thereof and thereby controlling an oscillation frequency.

Claim 14. (previously presented): The oscillator circuit in claim 2, wherein said variable capacitance element comprises a MOSFET.

Claim 15. (previously presented): The oscillator circuit in claim 2, wherein said control voltage generation circuit detects a phase difference between a divided signal of a signal generated by said oscillating unit and the reference signal, and outputs a control voltage according to the phase difference.

Claim 16. (previously presented): The oscillator circuit in claim 2, wherein said control voltage generation circuit is a PLL synthesizer circuit comprising a programmable counter, a

phase detection circuit comparing phases between a signal outputted from the programmable counter and the reference signal, and a low-pass filter blocking a high frequency component of an output signal of the phase detection circuit and outputting a DC control voltage to said oscillating unit.

Claim 17. (previously presented): The oscillator circuit in claim 2, wherein said divider circuit includes a divider circuit having a duty ratio of 50%.

Claim 18. (previously presented): The oscillator circuit according to claim 1, wherein the PLL synthesizer comprises a programmable counter configured to divide the frequency of the output signal of the voltage controlled oscillator having the frequency of n times of the target frequency, and wherein the phase detector detects the phase difference between signals divided by the programmable counter and the reference signal.

Claim 19. (previously presented): An oscillator circuit according to claim 1, wherein the output of the frequency divider is input to a mixing circuit where the output of the frequency divider is mixed with a received signal thereby converting the frequency of the received signal into a predetermined frequency.

Claim 20. (previously presented): An oscillator circuit according to claim 2, wherein the output of the second frequency divider is input to a mixing circuit where the output of the frequency divider is mixed with a received signal thereby converting the frequency of the received signal into a predetermined frequency.